FIG. 1

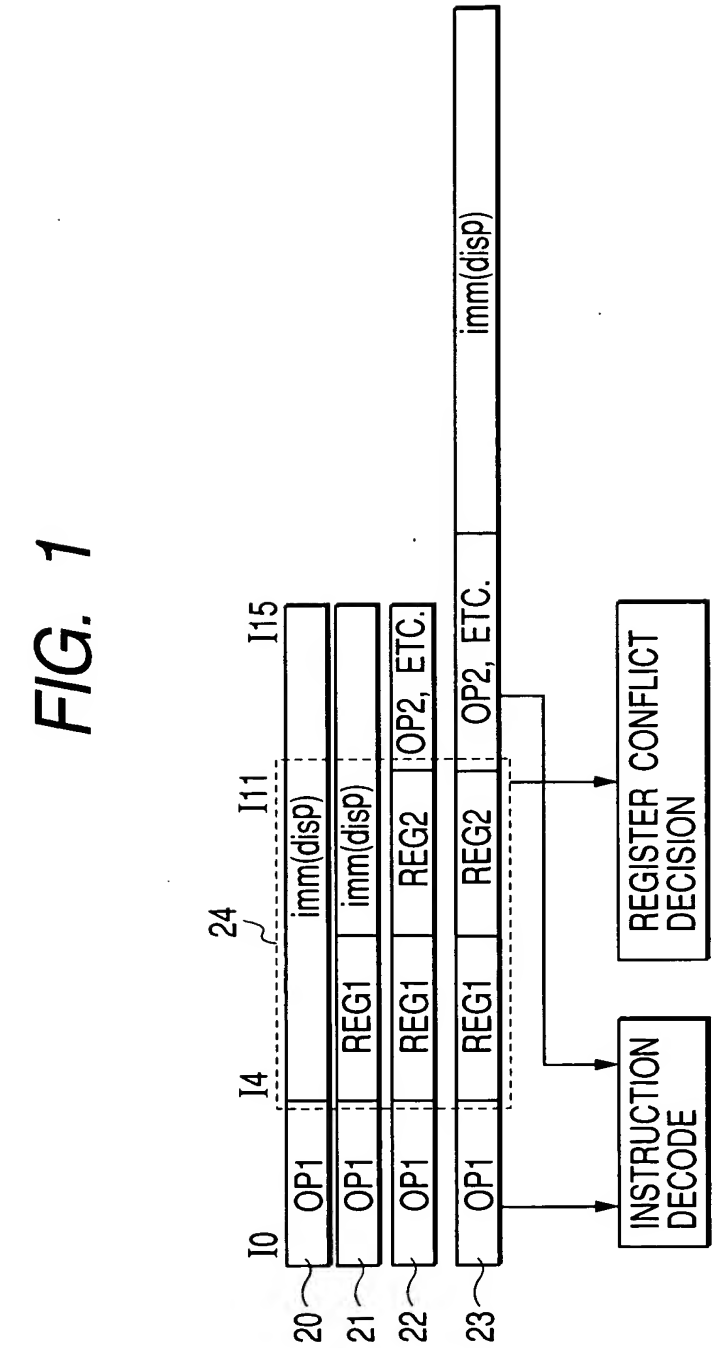

I0
I4
I11
I15
24
OP1
REG1
imm(disp)
OP2, ETC.
REG2
20
21
22
23
INSTRUCTION DECODE
REGISTER CONFLICT DECISION

FIG. 2

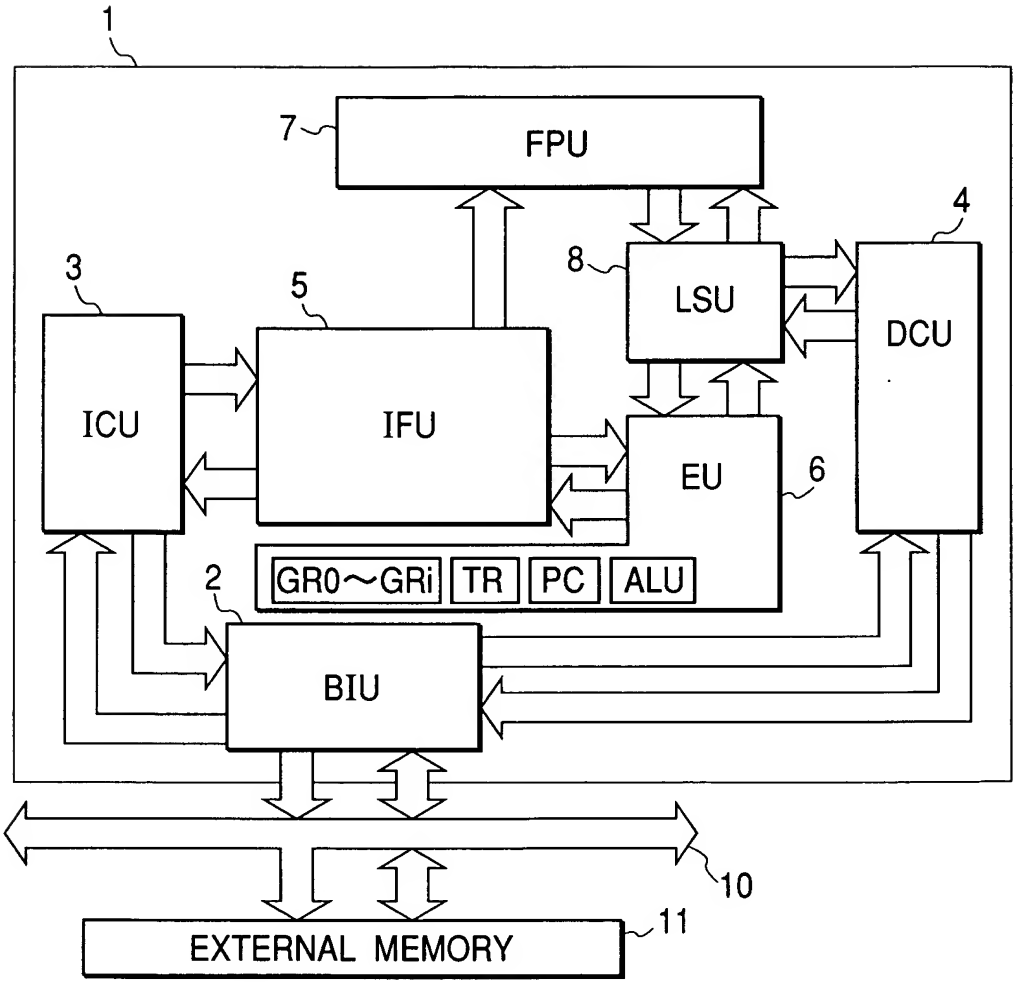
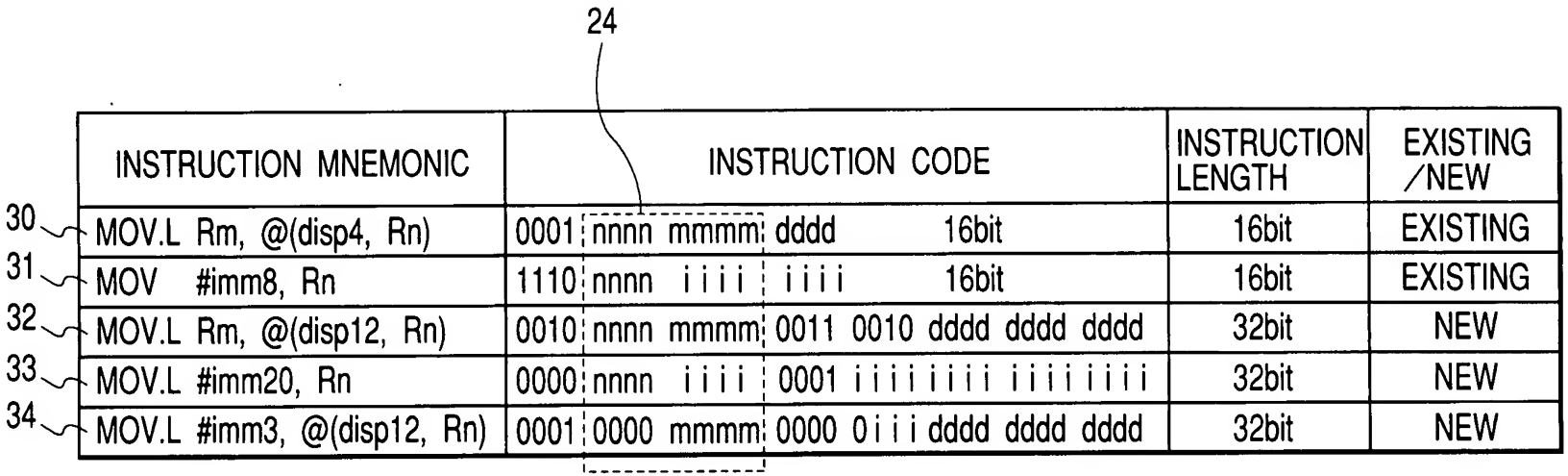

1
7
FPU
4
8
LSU
DCU
3
5
ICU
IFU
EU
6
GR0～GRi
TR
PC
ALU
2
BIU
10
11
EXTERNAL MEMORY

FIG. 3



	INSTRUCTION MNEMONIC	INSTRUCTION CODE	INSTRUCTION LENGTH	EXISTING /NEW
30	MOV.L Rm, @(disp4, Rn)	0001 nnnn mmmm dddd 16bit	16bit	EXISTING
31	MOV #imm8, Rn	1110 nnnn iiii iiii 16bit	16bit	EXISTING
32	MOV.L Rm, @(disp12, Rn)	0010 nnnn mmmm 0011 0010 dddd dddd dddd	32bit	NEW
33	MOV.L #imm20, Rn	0000 nnnn iiii 0001 iiiiiiii iiiiiiii	32bit	NEW
34	MOV.L #imm3, @(disp12, Rn)	0001 0000 mmmm 0000 0iii dddd dddd dddd	32bit	NEW

FIG. 4

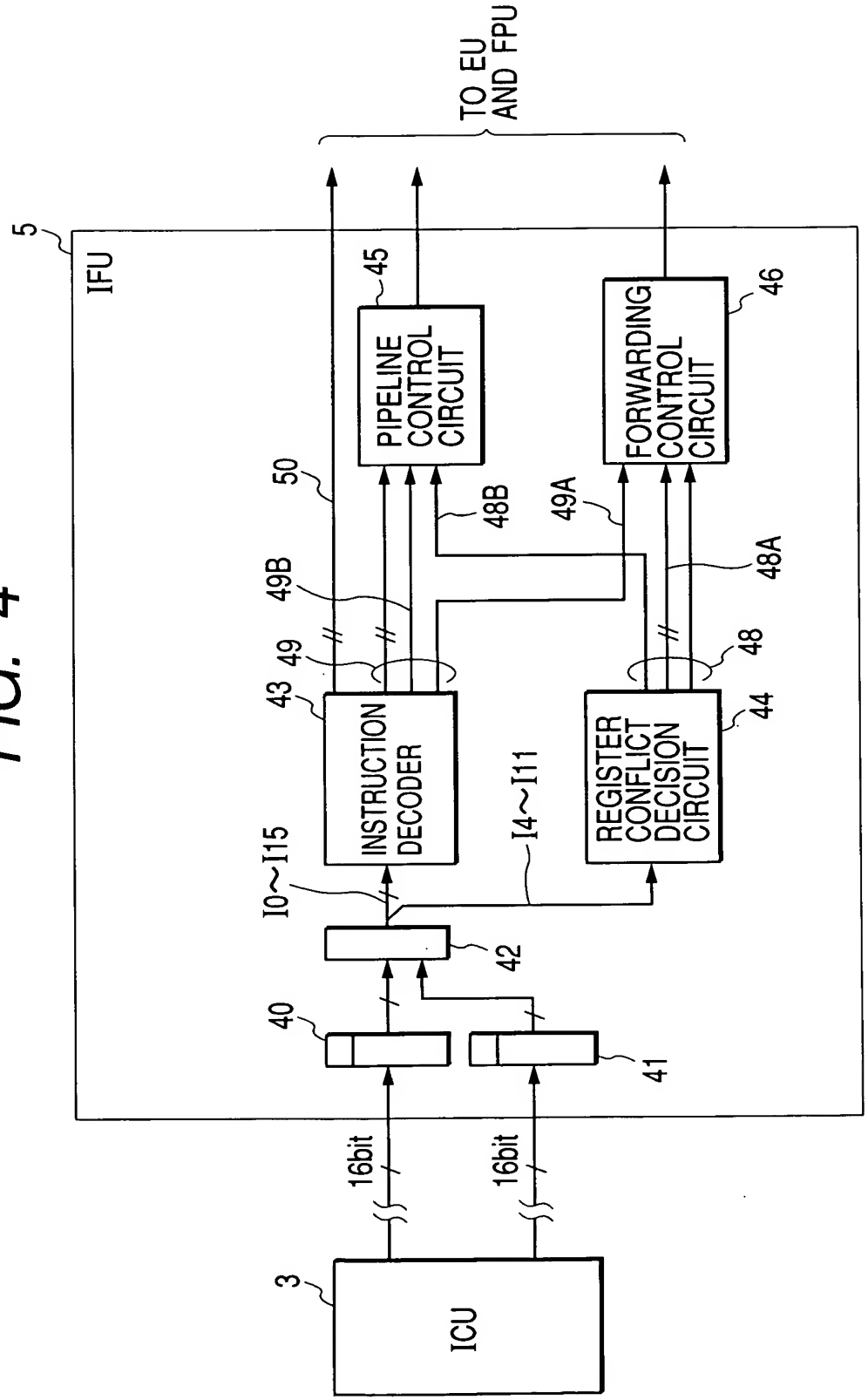

TO EU AND FPU
5
IFU
45
PIPELINE CONTROL CIRCUIT
46
FORWARDING CONTROL CIRCUIT
50
48B
49A
49B
48A
49
48
43
INSTRUCTION DECODER
REGISTER CONFLICT DECISION CIRCUIT
44
I0~I15
I4~I11
42
40
41
16bit
16bit
3
ICU

FIG. 5

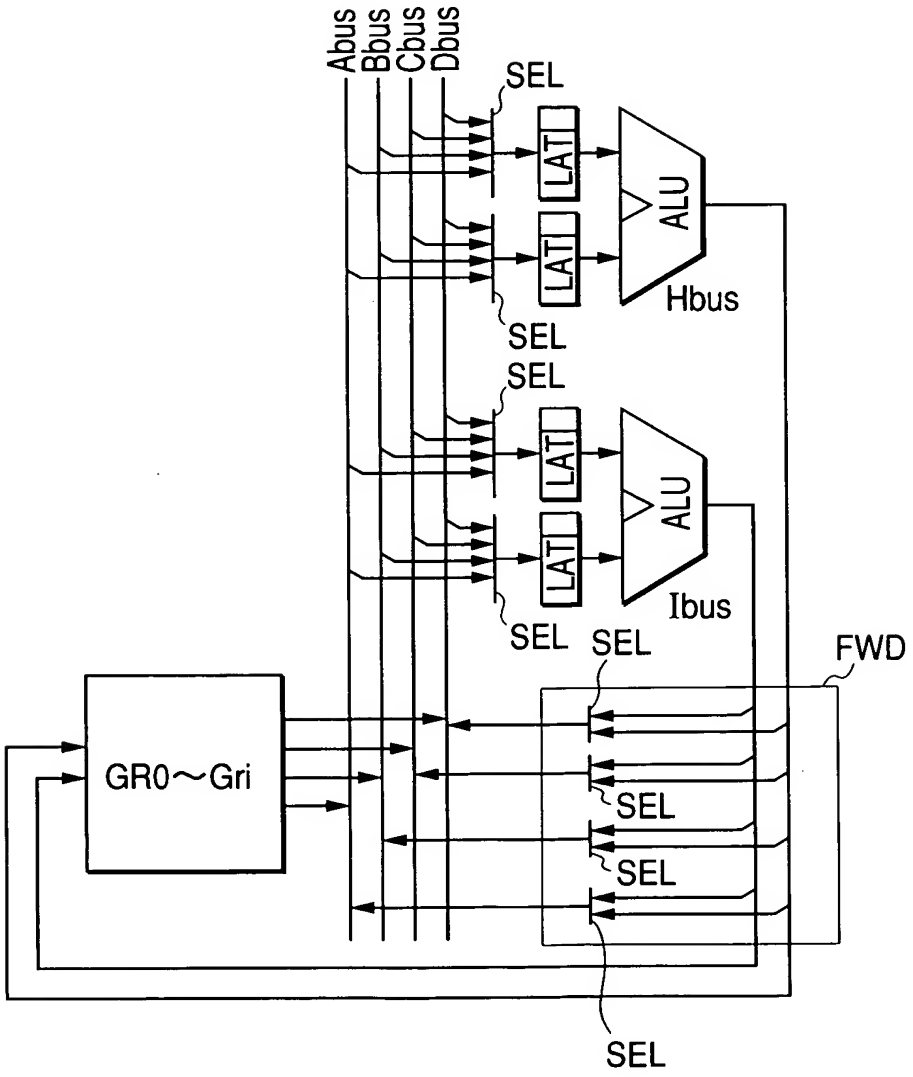

Abus
Bbus
Cbus
Dbus
SEL
LAT
ALU
Hbus
SEL
SEL
LAT
ALU
Ibus
SEL
SEL
FWD
GR0～Gri
SEL
SEL
SEL

FIG. 6

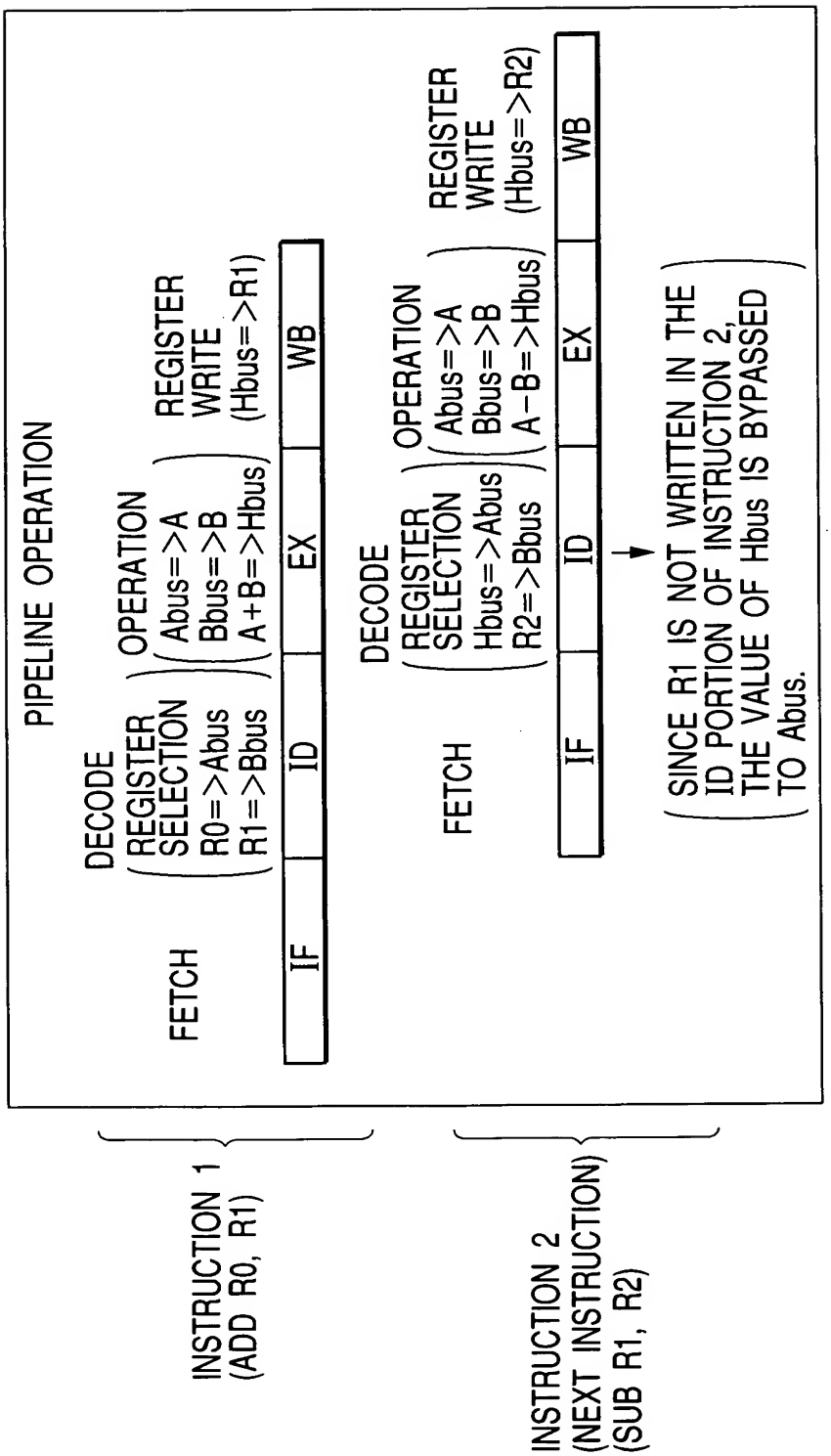

PIPELINE OPERATION
INSTRUCTION 1
(ADD R0, R1)
FETCH
DECODE
REGISTER SELECTION
R0=>Abus
R1=>Bbus
OPERATION
Abus=>A
Bbus=>B
A+B=>Hbus
REGISTER WRITE
(Hbus=>R1)
IF
ID
EX
WB
INSTRUCTION 2
(NEXT INSTRUCTION)
(SUB R1, R2)
FETCH
DECODE
REGISTER SELECTION
Hbus=>Abus
R2=>Bbus
OPERATION
Abus=>A
Bbus=>B
A−B=>Hbus
REGISTER WRITE
(Hbus=>R2)
IF
ID
EX
WB
(SINCE R1 IS NOT WRITTEN IN THE ID PORTION OF INSTRUCTION 2, THE VALUE OF Hbus IS BYPASSED TO Abus.)

FIG. 7

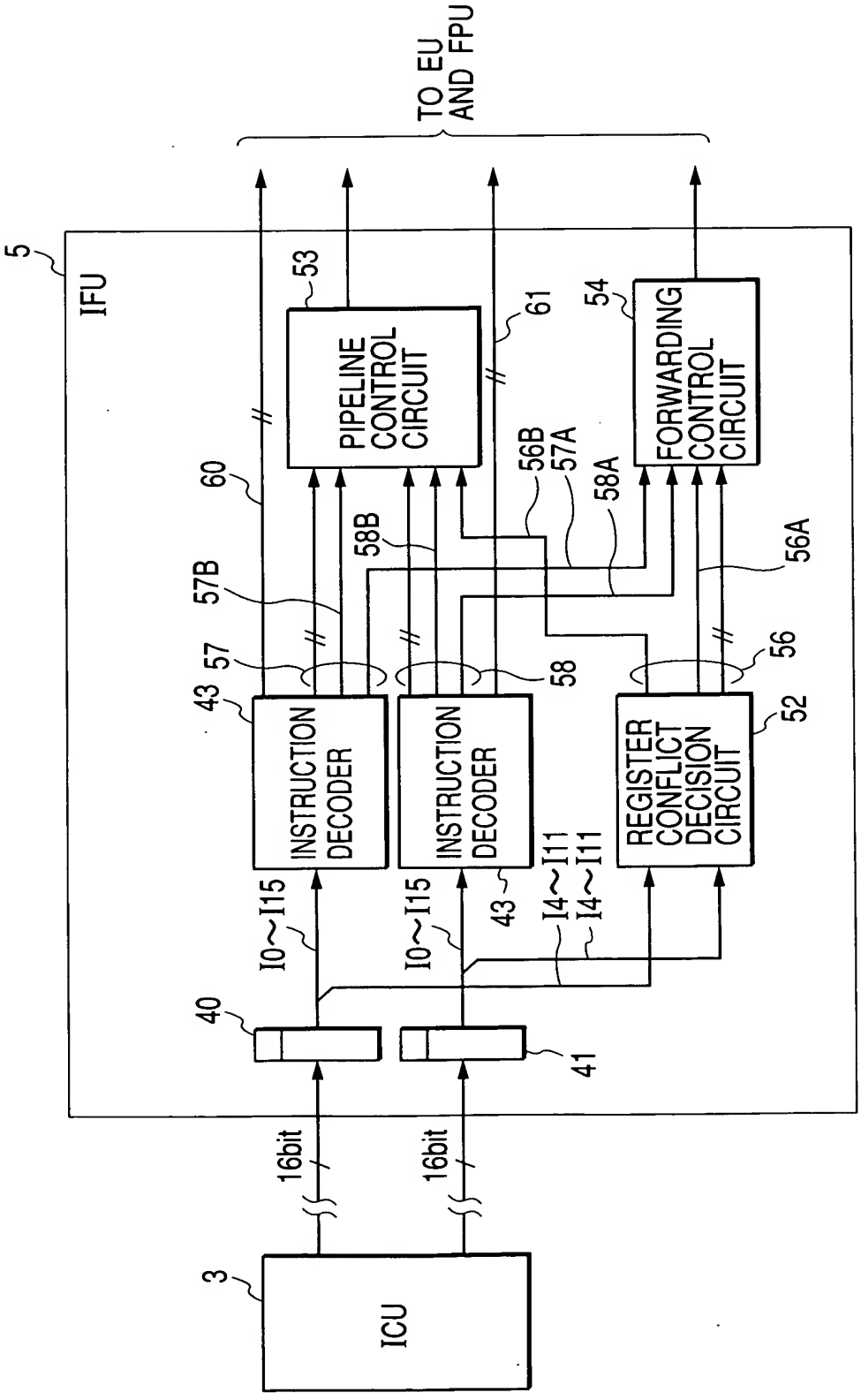

TO EU AND FPU
5
IFU
53
PIPELINE CONTROL CIRCUIT
61
54
FORWARDING CONTROL CIRCUIT
60
56B
57A
58A
58B
56A
57B
57
58
56
43
INSTRUCTION DECODER
INSTRUCTION DECODER
REGISTER CONFLICT DECISION CIRCUIT
52
I0~I15
I0~I15
43
I4~I11
I4~I11
40
41
16bit
16bit
3
ICU

FIG. 8

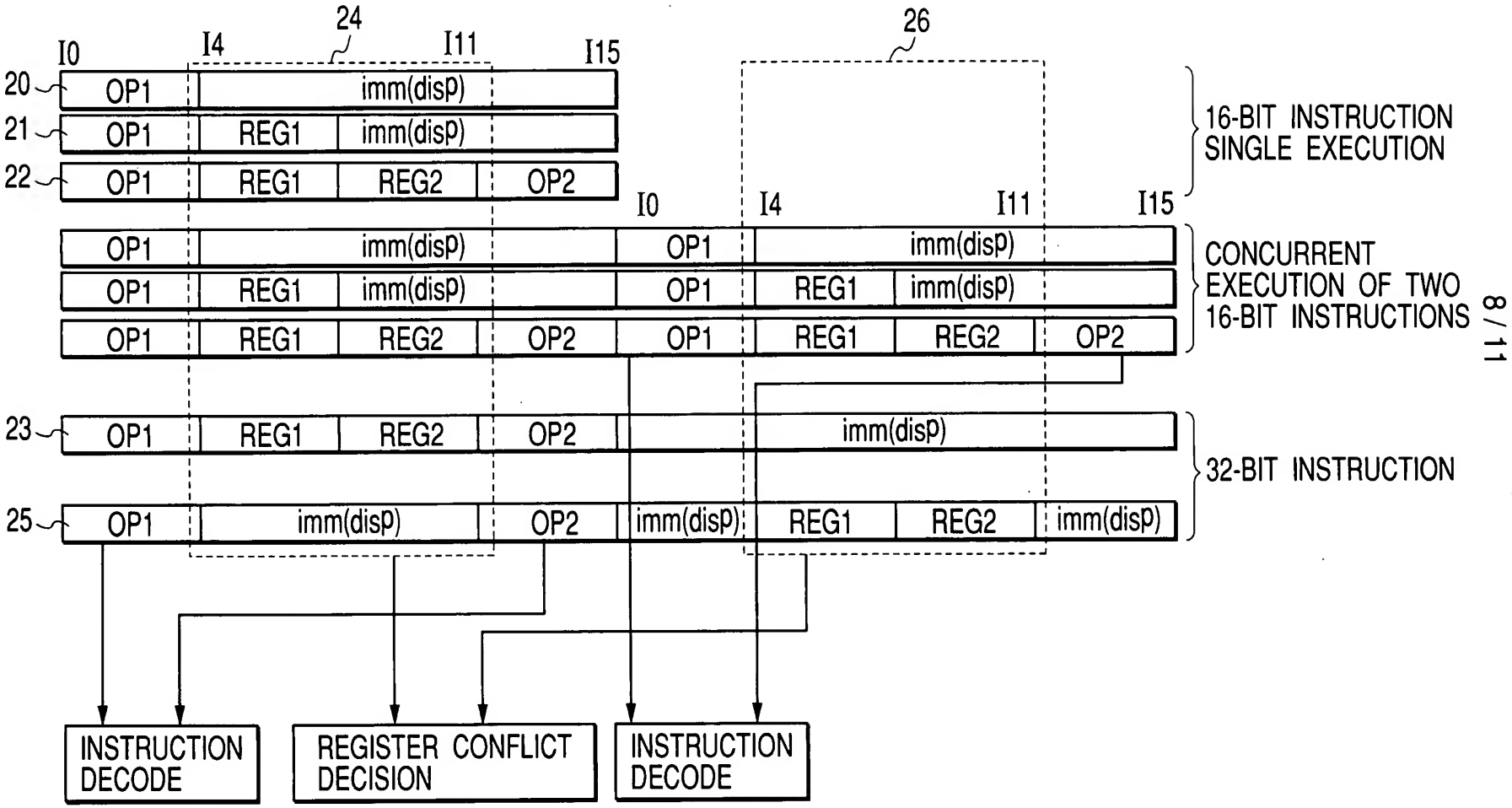

24
26
I0
I4
I11
I15
20
21
22
OP1
imm(disp)
REG1
REG2
OP2
16-BIT INSTRUCTION SINGLE EXECUTION
CONCURRENT EXECUTION OF TWO 16-BIT INSTRUCTIONS
23
25
32-BIT INSTRUCTION
INSTRUCTION DECODE
REGISTER CONFLICT DECISION
INSTRUCTION DECODE

FIG. 9

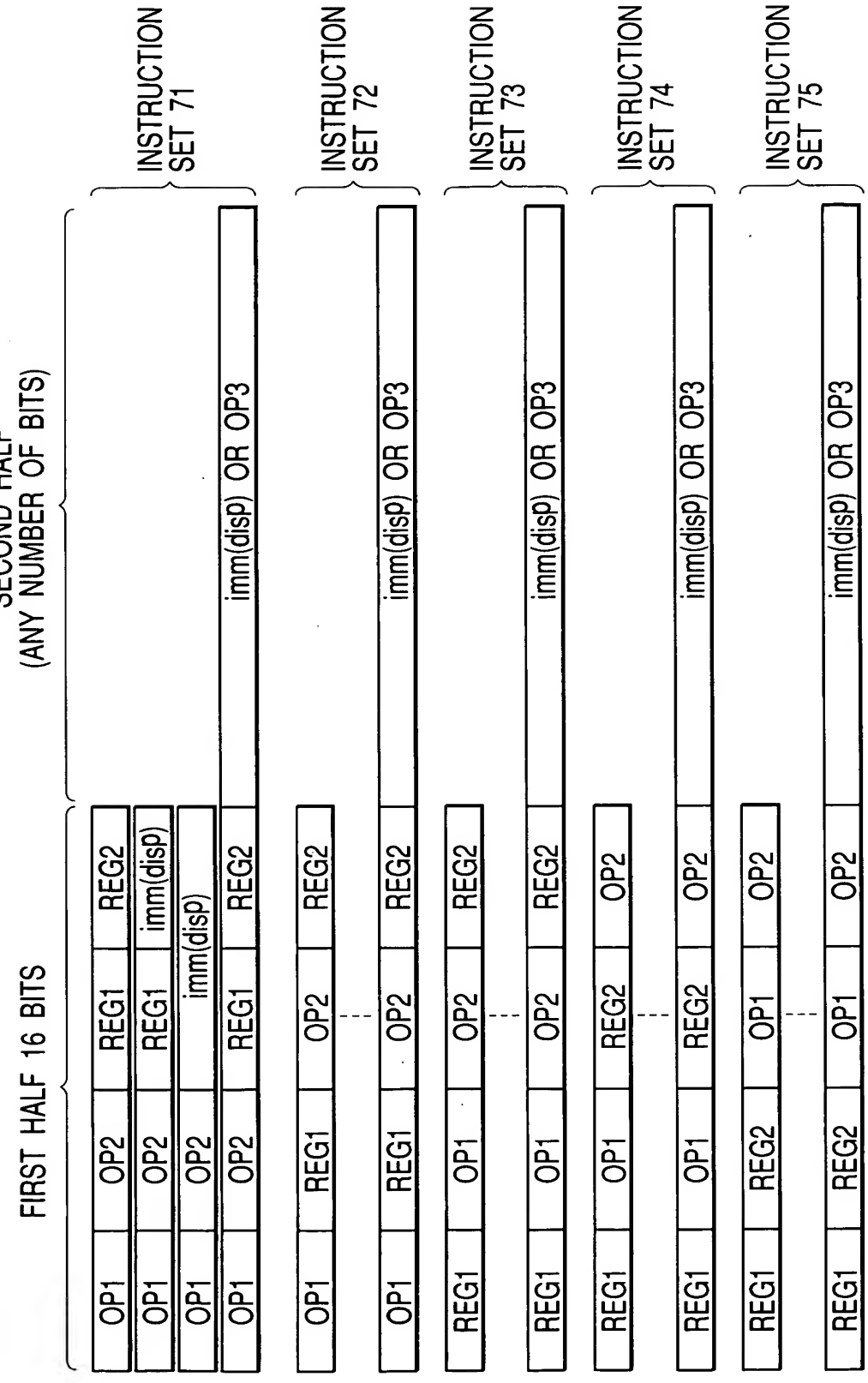

FIRST HALF 16 BITS
SECOND HALF
(ANY NUMBER OF BITS)
OP1
OP2
REG1
REG2
imm(disp)
imm(disp) OR OP3
INSTRUCTION SET 71
INSTRUCTION SET 72
INSTRUCTION SET 73
INSTRUCTION SET 74
INSTRUCTION SET 75

FIG. 10

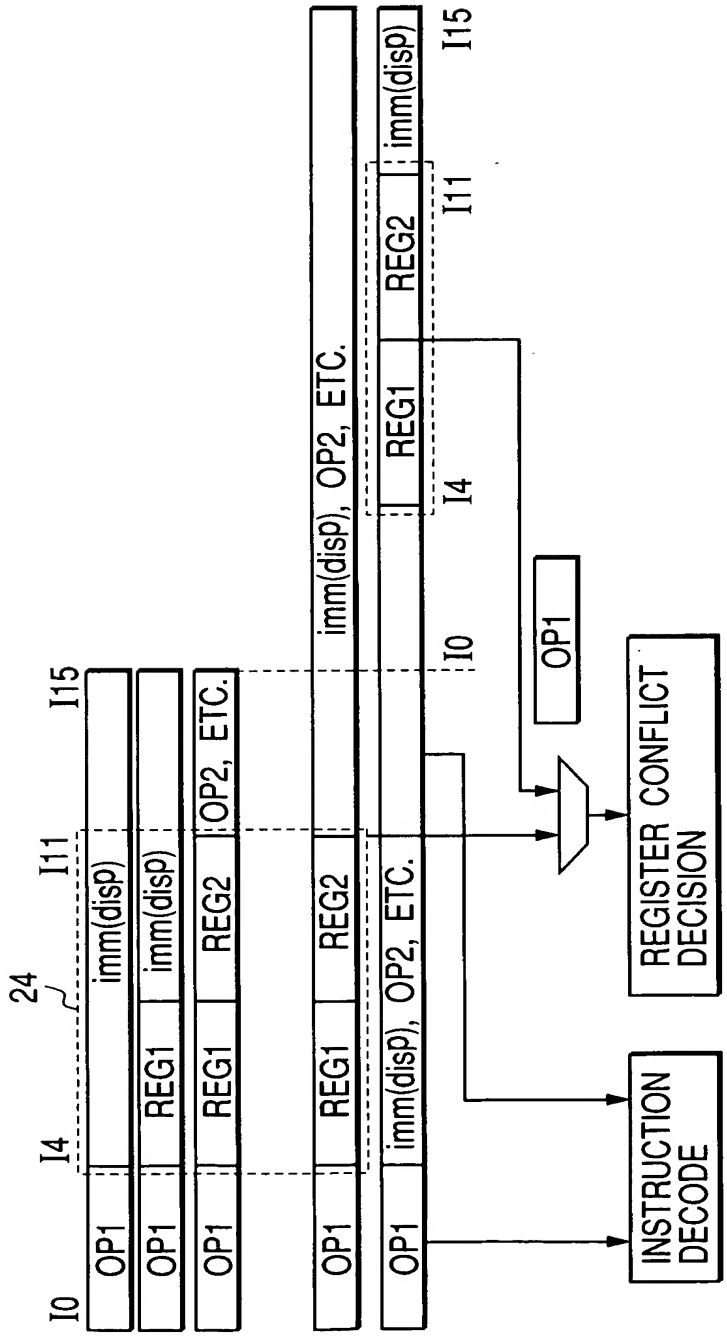
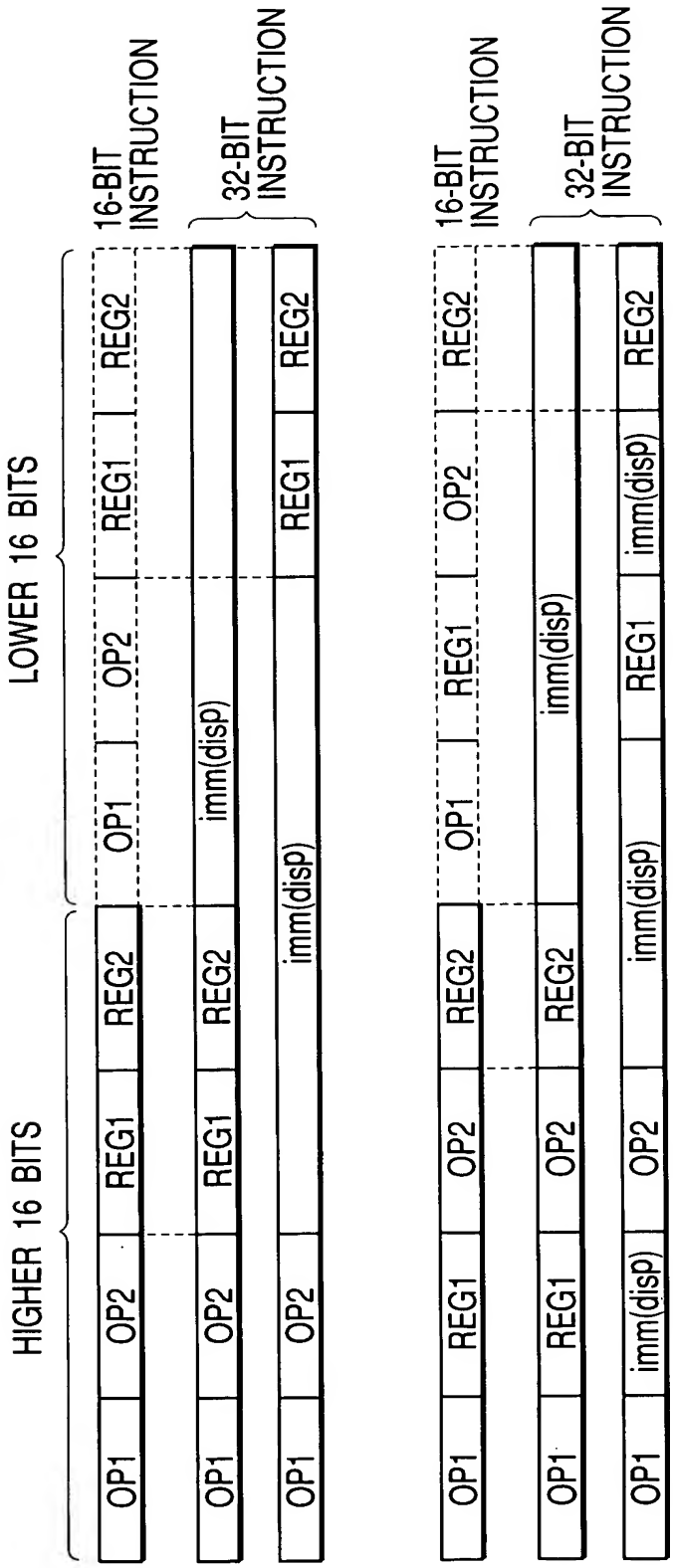

I0
I4
I11
I15
24
OP1
REG1
REG2
imm(disp)
OP2, ETC.
imm(disp), OP2, ETC.
INSTRUCTION DECODE
REGISTER CONFLICT DECISION

FIG. 11


HIGHER 16 BITS
LOWER 16 BITS
OP1
OP2
REG1
REG2
imm(disp)
16-BIT INSTRUCTION
32-BIT INSTRUCTION